CLAIM AMENDMENTS

The listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A data processing device, comprising an electronic memory component, the data processing device comprising:

~~at least two access-secured sub-areas, each having at least one assigned part of a parameter comprising at least one bit, the device configured such that an encryption method is applied to fewer than all of said sub-areas; and~~

an encryption block, ~~wherein~~ said encryption block receiving~~es~~ an address comprised of a series of parameters $a_0,\ldots,a_n$ and applying an encryption method on at least one ~~assigned part of said parameter from at least one of said sub-areas and encrypts said part of said~~ parameter to produce an encrypted series of parameters $a'_0,\ldots,a'_n$ according to the series:

$$a'_j = \begin{cases} f_{n-j+1}(a_j) & j = n \\ f_{n-j+1}\left(a_j + f_{n-j}(a_{j+1})\right) & j = 0,\ldots,n-1 \end{cases}$$

wherein encryption function f_{j+1} and encryption function f_j are distinct for all values of j, and

for at least a first parameter in said series of parameters, $a'_x \neq a_x$ and for at least a second parameter in said series of parameters, $a'_y = a_y$.

2-3. (Canceled)

4. (Previously Presented) The data processing device as claimed in claim 1, wherein the memory component comprises:

an erasable programmable read only memory,

an electrically erasable programmable read only memory or

a flash memory.

5. (Canceled)

6. (Currently Amended) A method of securing access to an electronic memory, comprising:

receiving, by a data processing device, an address comprised of a series of parameters $a_0,\ldots,a_n$ ~~, wherein the parameter is comprised of at least two parts, each part comprising at least one bit~~;

~~assigning, by said data processing device, said parts of the parameter into at least two access secured sub-areas located in said data processing device;~~ and

encrypting, by said data processing device, at least one of said ~~parts of the~~ parameters ~~in said access secured sub-areas~~ with an encryption method, ~~wherein said encryption method is applied to fewer than all of said sub-areas~~ to produce an encrypted series of parameters $a'_0,\ldots,a'_n$ according to the series:

$$a'_j = \begin{cases} f_{n-j+1}(a_j) & j = n \\ f_{n-j+1}\left(a_j + f_{n-j}(a_{j+1})\right) & j = 0,\ldots,n-1 \end{cases}$$

wherein encryption function f_{j+1} and encryption function f_j are distinct for all values of j, and

for at least a first parameter in said series of parameters, $a'_x \neq a_x$ and for at least a second parameter in said series of parameters, $a'_y = a_y$.

7. (Canceled)

8. (Currently Amended) The method as claimed in ~~claim 7~~ claim 6, characterized in that the function is one-to-one, according to the equation $a'_0 = f_{n+1}\left(a_0 + f_n\left(a_1 + f_{n-1}\left(a_2 + \ldots + f_1\left(a_n\right)\right)\right)\right)$.

9. (Canceled)

10. (Currently Amended) The~~A~~ data processing device of claim 1, ~~comprising an electronic memory component, comprising:~~

~~at least two access secured sub-areas, each having at least one assigned part of a parameter comprising at least one bit, the device configured such that an encryption method is applied to fewer than all of said sub-areas,~~ wherein the data processing device is utilized in at least one of:

a one smart card controller,

a reader integrated circuit,

a cryptography chipset, or

for application in at least one of audio or video encryption.

11-16. (Canceled)